Bit Range	Default & Access	Field Name (ID): Description
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.